REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Rejections under 35 U.S.C. §112

Claims 6 and 9 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, Applicant has cancelled claims 6 and 9 and respectfully requests reconsideration and withdrawal of the rejection.

2. Rejections of claim 1-9 under 35 U.S.C. §103(a)

With respect to the rejection of claims 1-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Jay (US 6,400,683) in view of Haywood (US 6,987,775) and Oldak (newly cited US 7,085,236), and to the rejection of claims 7-9 under 35 U.S.C. §103(a) as being patentable over Jay, Haywood, Oldak, and Tokura, Applicant respectfully traverses the rejections at least for the reason that Jay, Haywood, Oldak, and Tokura, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims.

In a controlling method and a control device according to the present inventions, a jitter buffer (FIFO) is set with a packet delete area, a packet add area, and a clock control area. The packet add area has a upper limit (T1). The packet delete area has a lower limit (T4). The clock control area has a lower limit (T2) and an upper limit (T3). The upper limit (T1) of the packet add area is lower than the lower limit (T2) of the clock control area. The lower limit (T4) of the packet delete area is high than the upper limit (T3) of the clock control area. Accordingly, even if packet data quantity in the jitter buffer exceeds the upper limit (T3) of the clock control area, the packet data is not deleted at once. And, even if packet data quantity in the jitter buffer falls below the lower limit (T2) of the clock control area, the packet data is not added at once.

Accordingly, the present invention has advantages as described in the specification, particularly in page 6, lines 22 to page 7, line 18.

In contrast with Applicant's claimed invention, Jay merely shows to control clock frequency according to stored state of a buffer. Jay does not teach, disclose, or suggest that the buffer is set is set a packet delete area, a packet add area, and a clock control area, and that a relationship between limits of the packet delete areas and packet add area and limits of the clock control area as recited Applicant's claimed invention.

With respect to Haywood, the reference generally shows variable FIFO that is comprised with three memories 16, 17 and 18. However, Haywood does not teach, disclose, or suggest that a FIFO is set is set a packet delete area, a packet add area, and a clock control area, and that a relationship between limits of the packet delete area and packet add area and limits of the clock control area. As previously submitted in the Response filed September 15, 2008, Applicant respectfully reiterates that Haywood's variable size FIFO memory with head and tail caching is completely different in structure and function from Applicant's claimed features.

Further, as previously submitted, with respect to Jay's controlling clock frequency based on buffer level, Applicant respectfully reiterates that Jay is similar to a conventional method discussed in page 2 of the original specification, and that, even if Jay were combined with Haywood, the combination would still fail to arrive at Applicant's claimed invention, which includes controlling a stored packet quantity of the FIFO to delete a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, and controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area, as recited claim 1.

With respect to Oldak, Applicant respectfully asserts that Oldak does not teach, disclose, or suggest that a relationship between limits of the packet delete area and packet add area and limits of the clock control area.

According to Examiner-cited col. 5, lines 17-31 of Oldak, the following is disclosed:

> *"Congestion is typically handled using queue management. One queuing method is referred to as first-in-first-out (FIFO) queuing. In FIFO queuing, arriving packets get dropped when a queue is full, regardless of flow or importance. An improvement in FIFO queuing is referred to as*

> *"Drop-Tail." In drop-tail, when a router's queue (also referred to as a buffer) is filled, i.e., when incoming packets come faster than the router's capacity to output packets, all additional packets are discarded because there is no place to store the additional packets. In the drop-tail scheme, TCP senders are generally on the lookout for acknowledgements (ACKs) from a receiver that indicate such drops, and cut their send rate in such a case. Thus, drop-tail signals congestion only when the queue is already saturated, is likely to drop more packets from the same flow, and is unfair with bursty flows."* [emphasis added]

In view of Oldak's disclosure of discarding additional incoming packets as there is no place to store the additional packets, Applicant respectfully asserts that Oldak clearly does not particularly teach, disclose, or suggest raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area, lowering the clock frequency when the stored packet quantity of the FIFO reaches a lower limit of the clock control area, and setting the clock control area between the packet add area and the packet delete area so as to control a stored packet quantity of the FIFO as recited in, e.g., claim 1 of the present invention.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03, are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Further, according to MPEP §2141(I), Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case. The Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

Moreover, according to MPEP §2141(II), when applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.

As Jay, Haywood, and Oldak, combined or separately, fail to teach, disclose, or suggest each and every feature of claims 1, 2, and 5, the obviousness rejection is improper.

With respect to the rejection of claims 7-8, Applicant respectfully asserts that the arguments set forth above in relation to the rejection of claim 1 are also applicable to dependent claims 7-8, and that Tokura, alone or in combination with Jay, Haywood, and Oldak, still fails to teach, disclose, or suggest each and every feature of the claimed invention.

Tokura merely show a controlling of the packet transfer rate. However, Tokura does not teach, disclose, or suggest that a relationship between limits of the packet delete area and packet add area and limits of the clock control area.

As previously submitted, Tokura generally describes a method for packet transfer that is controlled by using an acceleration rate of packet transfers. However, similar to Jay and Haywood, Tokura also fails to teach, disclose, or suggest controlling a stored packet quantity of the FIFO to delete a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area, and to delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, and controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to add the packets when the stored packet quantity falls below a lower limit of the packet add area, as recited in amended claim 1.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to follow tenets A-D in relying on Haywood, Jay, and Tokura in the obviousness rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 1-9.

3. Rejections of claims 10-15 under 35 U.S.C. §103(a)

With respect to the rejection of independent claim 10 directed to a device and its dependent claims 12-15 under 35 U.S.C. §103(a) as being unpatentable over Jay and Haywood in view of Suzuki (U.S. 2002/0009054) or Oltean (US 6,044,113), Applicant respectfully traverses the rejection at least for the reasons set forth above with respect to method claims 1-6, which parallel the device claims, over Jay and Haywood, and for the reason that Suzuki and Oltean also fail to cure the deficiencies of Jay and Haywood.

As previously submitted, Suzuki generally shows to control a delay time. More specifically, Suzuki shows controlling a delay time of a packet by using a delay unit 103 in a device and method for reducing delay jitter in data transmission. Applicant respectfully asserts that there is no teaching, disclosure, or suggest in Suzuki of a FIFO, having an input side and an output side, that configures the jitter buffer, a packet deletion circuit provided on the input side of the FIFO, a packet addition circuit provided on the output side of the FIFO, a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO, a VCO that supplies to vary a reproduced clock frequency, and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof, wherein the buffer control circuit controls the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, and the buffer control circuit controls to add the packets when the stored packet quantity falls below an upper limit of a packet add area, and a decoder that accepts the packets outputted from the packet addition circuit, and decodes frames of the packets based on the clock frequency supplied from the VCO, as recited in amended claim 10 and its dependent claims.

Oltean, on the other hand, generally describes a digital pulse with modulator, which is completely different subject matter than the presently claimed invention and has no resemblance structurally or functionally to Applicant's device recited in claim 10 and its dependent claim 11.

Further, even if Suzuki or Oltean were combined with Jay and Haywood, the combination would still fails to include at least a packet deletion circuit provided on the input side of the FIFO, a packet addition circuit provided on the output side of the FIFO, a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO, as recited in claim 10.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to follow tenets A-D in relying on Haywood, Jay, Suzuki, and Oltean in the obviousness rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 10-15.

4. Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-2, 4-5, 7-8, and 10-15 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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